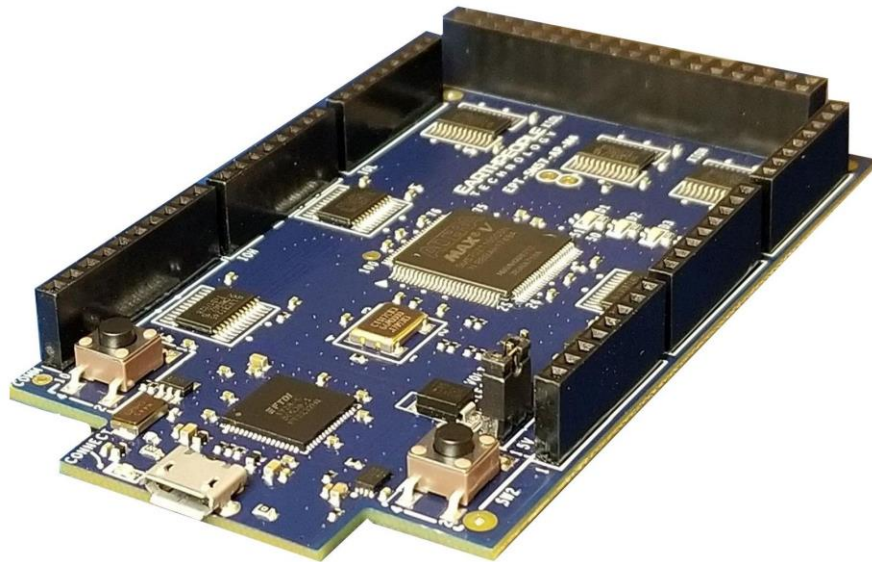


MegaMax CPLD Development System

Data Sheet



The MegaMax is a small form factor CPLD Development System. The core functions of the MegaMax are a two channel USB to Serial chip, 570 Logic Cell CPLD and thirty two Inputs/Outputs. The board is powered from a USB port. There is also three pin header to select either +3.3V or +5V for the I/O's.

The MegaMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin. So, the MegaMax can drive LEDs and sensors directly.

The MegaMax has the following features:

- Intel/Altera 5M570 CPLD with 440 Macrocells
- 66 MHz oscillator for driving USB data transfers and users code
- Three bidirectional voltage translator/bus transceivers
- 32 user Input/Outputs available as five 8 bit ports
- Ports have jumper selectable 3.3V/5 Volt Input/Output
- Four Green LED's accessible by the user
- Two PCB switches accessible by the user

1 Block Diagram

Figure 1-1 MegaMax Component Location

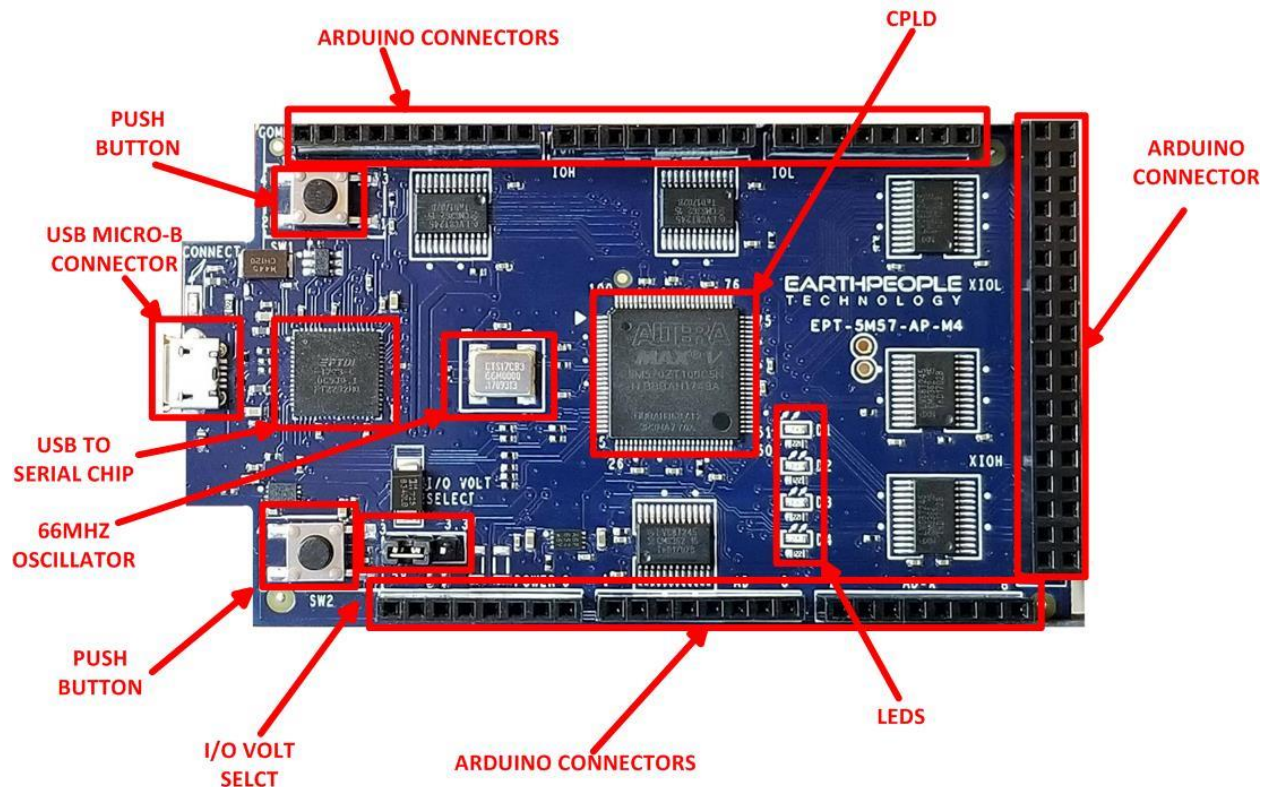
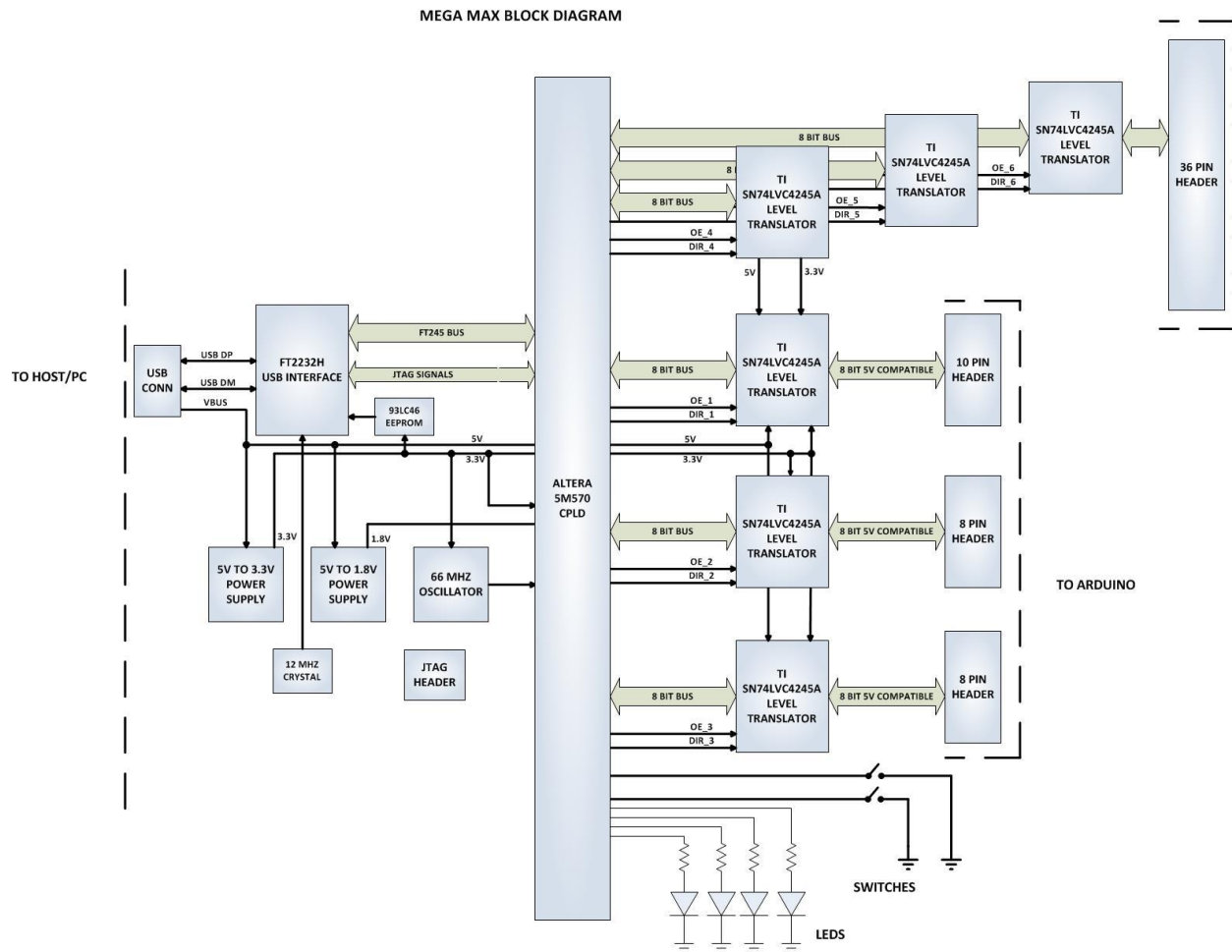
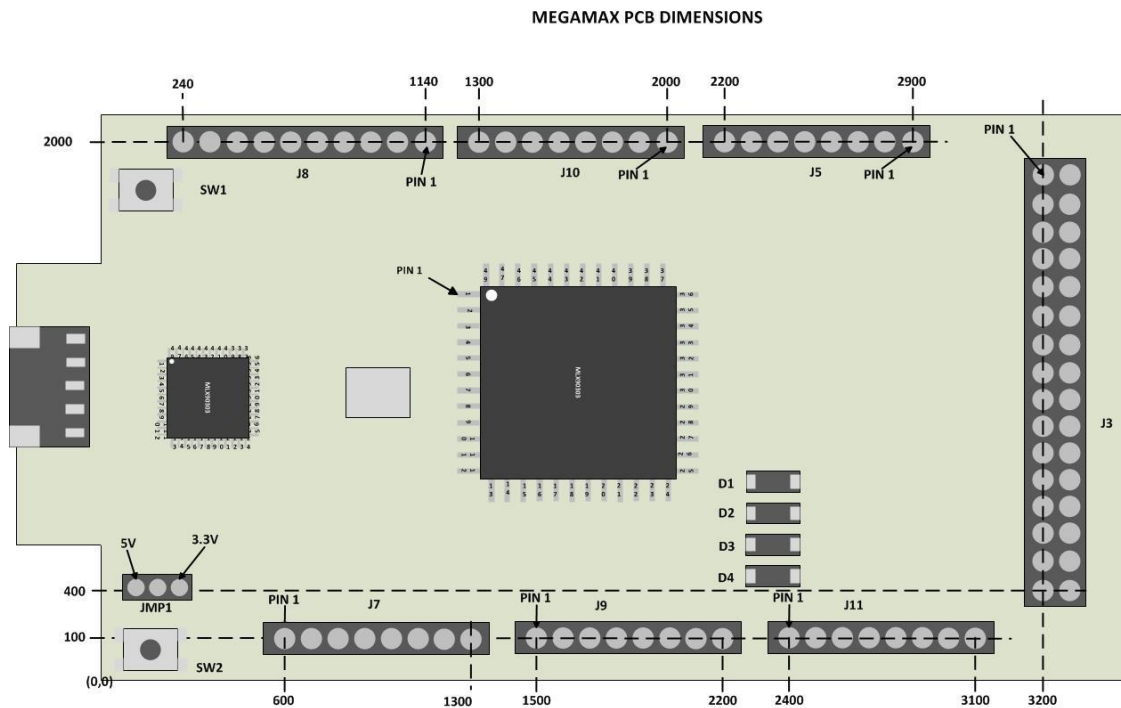


Figure 1-2 MegaMax Block Diagram



2 Mechanical Dimensions

Figure 2-1 MEgaMax Mechanical Dimensions



All dimensions in mils (0.001")

1 Pin Mapping

Figure 3-1. Pin Mapping between Connectors, MAXV CPLD and User code

Component	Pin	Net Name	Pin on CPLD	Signal in EPT Project Pinout
66MHz Oscillator	3	GCLK	12	aa[1]
Reset	2	NA	44	aa[0]
U12	16	AD0	24	JTAG_TCK (Not In Project)

CPLD Development System Data Sheet

	17	AD1	23	JTAG_TDI (Not In Project)
	18	AD2	25	JTAG_TDO (Not In Project)
	19	AD3	22	JTAG_TMS (Not In Project)
	38	BD0	19	BD_INOUT0
	39	BD1	18	BD_INOUT1
	40	BD2	17	BD_INOUT2
	41	BD3	16	BD_INOUT3
	43	BD4	15	BD_INOUT4
	44	BD5	14	BD_INOUT5
	45	BD6	7	BD_INOUT6
	46	BD7	6	BD_INOUT7
	48	BC0	5	BC_IN1
	52	BC1	4	BC_IN0
	53	BC2	3	BC_OUT2
	54	BC3	2	BC_OUT1
	55	BC4	1	BC_OUT0
SW1	1	SW_USER_1	20	SW_USER_1
SW2	1	SW_USER_2	21	SW_USER_23
U7	2	TR_DIR_1	100	TR_DIR_1
U4	2	TR_DIR_2	29	TR_DIR_2

CPLD Development System Data Sheet

U5		2	TR_DIR_3	85	TR_DIR_3
U15		2	TR_DIR_4	30	TR_DIR_4
U13		2	TR_DIR_5	27	TR_DIR_5
U7		22	TR_OE_1	86	TR_OE_1
U4		22	TR_OE_2	28	TR_OE_2
U5		22	TR_OE_3	74	TR_OE_3
U15		22	TR_OE_4	73	TR_OE_4
U13		22	TR_OE_5	26	TR_OE_5
D1		1	LED_GR_1_N	54	LED0
D2		1	LED_GR_2_N	53	LED1
D3		1	LED_GR_3_N	52	LED2
D4		1	LED_GR_4_N	51	LED3
U7	3	21	LB0	87	LB_COMM0
	4	20	LB1	89	LB_ COMM 1
	5	19	LB2	91	LB_ COMM 2
	6	18	LB3	92	LB_ COMM 3
	7	17	LB4	96	LB_ COMM 4
	8	16	LB5	97	LB_ COMM 5
	9	15	LB6	98	LB_ COMM 6
	10	14	LB7	99	LB_ COMM 7
U4	3	21	LB8	33	LB_IO80
	4	20	LB9	34	LB_IO81

CPLD Development System Data Sheet

	5	19	LB10	35	LB_IO82
	6	18	LB11	36	LB_IO83
	7	17	LB12	38	LB_IO84
	8	16	LB13	40	LB_IO85
	9	15	LB14	41	LB_IO86
	10	14	LB15	42	LB_IO87
U5	3	21	LB16	81	LB_IO90
	4	20	LB17	82	LB_IO91
	5	19	LB18	83	LB_IO92
	6	18	LB19	84	LB_IO93
	7	17	LB20	78	LB_IO94
	8	16	LB21	77	LB_IO95
	9	15	LB22	76	LB_IO96
	10	14	LB23	75	LB_IO97
U13	3	21	LB24	47	LB_IOHA0
	4	20	LB25	48	LB_IOHA1
	5	19	LB26	49	LB_IOHA2
	6	18	LB27	50	LB_IOHA3
	7	17	LB28	55	LB_IOHA4
	8	16	LB29	56	LB_IOHA5
	9	15	LB30	57	LB_IOHA6
	10	14	LB31	58	LB_IOHA7

U15	3	21	LB32	61	LB_IOL0
	4	20	LB33	66	LB_IOL1
	5	19	LB34	67	LB_IOL2
	6	18	LB35	68	LB_IOL3
	7	17	LB36	69	LB_IOL4
	8	16	LB37	70	LB_IOL5
	9	15	LB38	71	LB_IOL6
	10	14	LB39	72	LB_IOL7
U14	3	21	LB40	64	LB_HB0
	4	20	LB41	62	LB_HB1
	5	19	LB42	43	LB_HB2
	6	18	LB43	44	LB_HB3

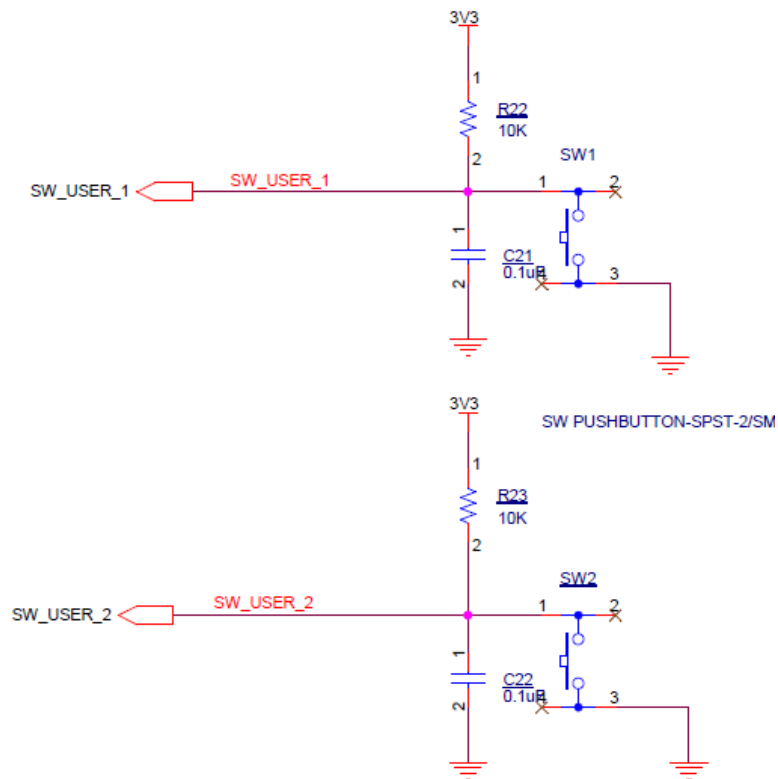
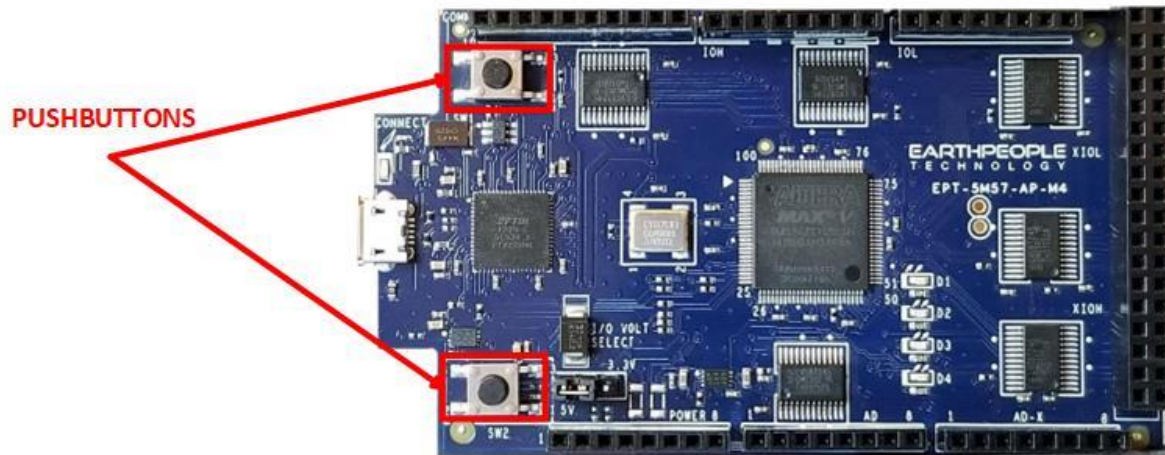
2 Pushbutton switches

The MegaMax includes two push button switches. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout
SW1	SW_USER_1	20	SW_USER_1
SW2	SW_USER_2	21	SW_USER_23

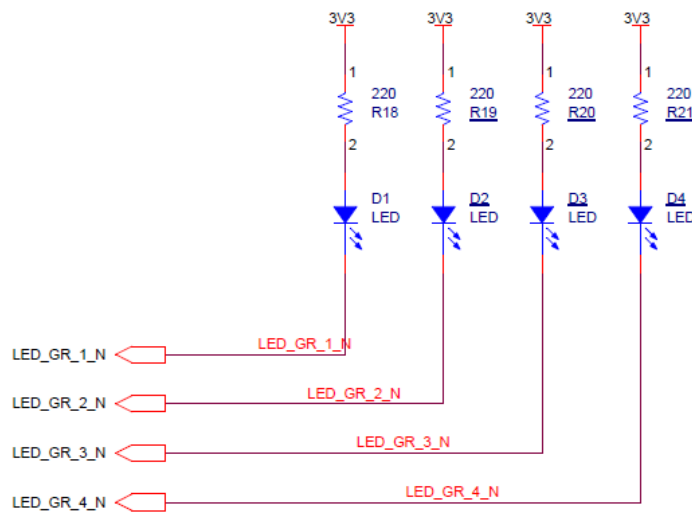


CPLD Development System Data Sheet



3 LEDs

The MegaMax includes four Green LEDs. The LEDs are connected to the CPLD in a “Current Sink” configuration. This means the LEDs Anodes are permanently connected to +3.3V. Each Cathode side of the LEDs are connected to an individual I/O of the CPLD. In order to turn on the LED, the CPLD I/O must apply a low signal. This will complete the LED drive circuit and current will flow through the LED. To turn the LED off, the CPLD I/O must either “float” or drive a high onto the pin.



Component	Net Name	Pin on FPGA	Signal in EPT Project Pinout
LED1	LED[1]	50	LED[0]
LED2	LED[2]	51	LED[1]
LED3	LED[3]	52	LED[2]
LED4	LED[4]	53	LED[3]



3 Host PC Connection

The MegaMax includes an LED that signifies the connection of the board with the Host PC. The connect LED has the word “CONNECT” in silkscreen next to the LED. This LED will only light up once the Host PC has correctly enumerated the USB device (FT232HQ chip). When this LED is lit up it can tell the user three things:

- Power has been applied to the MegaMax via USB
- The FT232HQ chip is working properly
- The Host PC has found the appropriate driver and will communicate with the MegaMax

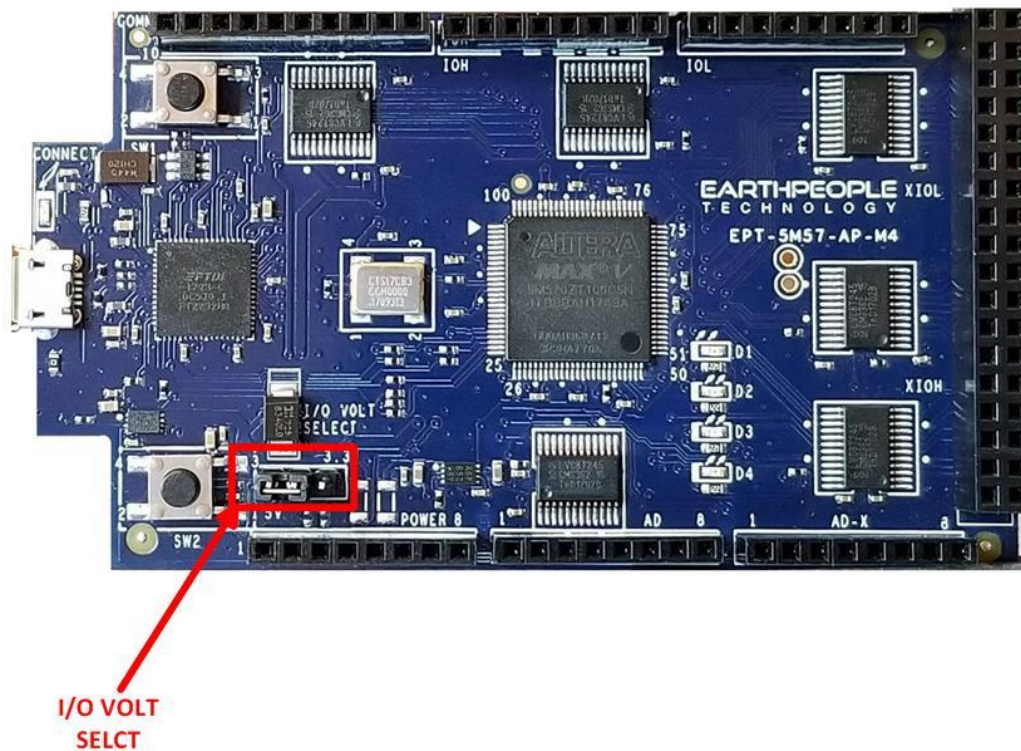
CONNECT LED



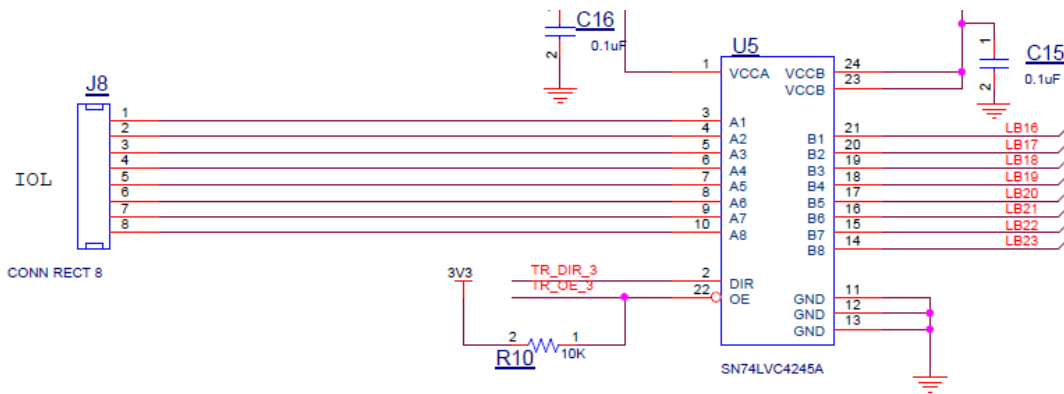
4 Inputs/Outputs

The UnoMax is designed from the ground up as a development board for beginners. All of the Inputs/Outputs are protected by the 74LVC8245 transceiver chips. These transceivers provide both voltage level translations and protection from over current and over voltage. The transceivers can sink up to 50mA per pin.

There are 24 Inputs/Outputs which are selectable between +3.3V and +5 Volt. JMP1 is used to select which voltage the 24 Inputs/Outputs are set to.



The I/O's are organized as three 8 bit directional ports. Each port must be defined as input or output. This means that all 8 bits of a port will point in the same direction, depending on the direction bit of the transceiver. The direction bit can be changed at any time, so that a port can change from input to output in minimum setup time of 6 nanoseconds. Each port also has an enable pin. This enable pin will enable or disable the bits of the port. If the port is disabled, the bits will “float”.



This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has VCCB, which is set at 3.3 V, and A port has VCCA, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, OE) is powered by VCCA.

3.1 Electrical Characteristics

for $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}^{(1)}$

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

for $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}^{(1)}$

			MIN	MAX	UNIT
V _{CCB}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CCB} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CCB} = 2.7 V to 3.6 V		0.8	V
V _{IB}	Input voltage		0	V _{CCB}	V
V _{OB}	Output voltage		0	V _{CCB}	V
I _{OH}	High-level output current	V _{CCB} = 2.7 V		−12	mA
		V _{CCB} = 3 V		−24	
I _{OL}	Low-level output current	V _{CCB} = 2.7 V		12	mA
		V _{CCB} = 3 V		24	
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

3.2 Timing Characteristics

 over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V},$ $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

3.3 Description

24 mA drive at 3-V supply

– Good for heavier loads and longer traces

 Low V_{IH}

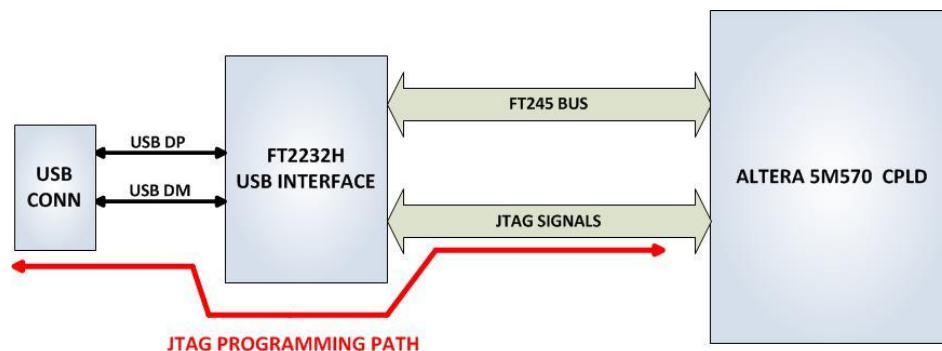
– Allows 3.3-V to 5-V translation

Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

5 MAXV Programming

The MegaMax uses the second channel of the FT2232H chip as a dedicated CPLD programming port. The CPLD must be programmed via JTAG signals and the FT2232H has built in JTAG signals.



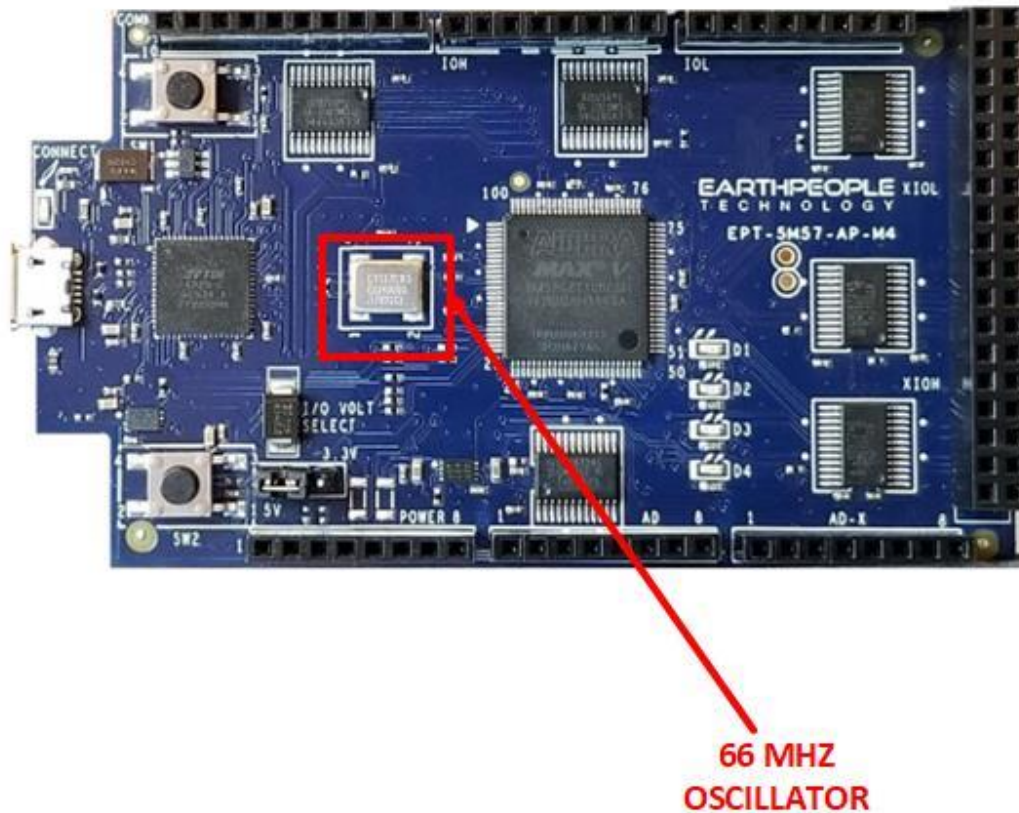
4 Oscillator

There is a 66MHz oscillator on the MegaMax, This oscillator has the following Vendor and P/N

1. 66MHz, Renesas Electronics America Inc; P/N: XLH536066.000000I

This oscillators are connected to the Global Clock inputs on the FPGA. Both devices provide stable clock for the FPGA's internal DLL's. The user can access these clock sources by calling the net connected to the FPGA pin.

Component	Net Name	Pin on CPLD	Signal in EPT Project Pinout	
66MHz Osc	GCLK1	23	CLK_66MHZ	



XLH536066.000000I

PARAMETERS	MAX (unless otherwise noted)
Frequency	66MHz

Supply Voltage (VDD)	3.3V
Input Current (IDD) >50.000 ~ 67.000MHz	25 mA
Standby Current	10 μ A
Output Symmetry (50% VDD) >50.000 ~ 170.000MHz	40% ~ 60%
Rise/Fall Time (10%/90% VDD Levels) (TR/TF) 1.000 ~ 80.000MHz	6 nS
Output Voltage (VOL) (VOH)	10% VDD 90% VDD Min
Output Load (HCMOS)	15 pF
Start-up Time (TS)	10 mS
Frequency Stability	± 25 ppm
Operating Temperature	-40°C ~ 85°C

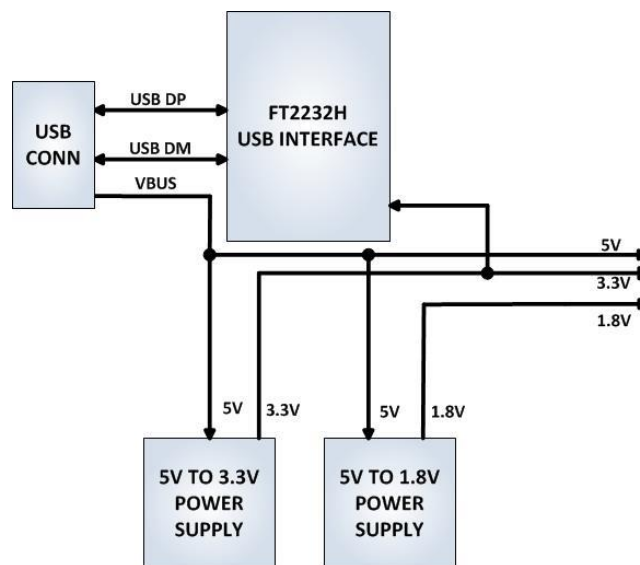
5 USB to Serial

The FT2232HQ is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC. The device features two interfaces that can be configured for asynchronous or synchronous serial or parallel FIFO interfaces. The two channels can also be independently configured to use an MPSSE engine. This allows the two ports of the FT2232HQ to operate independently as UART/Bit-Bang ports or MPSSE engines used to emulate JTAG, SPI, I2C, Bit-bang or other synchronous serial modes.

The chip is powered by +3.3V and includes an internal +1.8V regulator to power the chip core. It uses +3.3V I/O interfacing and is +5V Tolerant. Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface. Asynchronous serial UART interface option with full hardware handshaking and modem interface signals. Fully assisted hardware or X-On / X-Off software handshaking. UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.

6 MegaMax Power

The MegaMax is powered from the USB bus of a Host/PC. The USB supplies a maximum of +5V @ 500mA's. The components of the MegaMax must share this power with the user code that will run inside the CPLD along with any external power use.



1.1.1 Core Board Power Budget

Device	Part Number	+1.8V Power	+3.3V Power
--------	-------------	-------------	-------------

CPLD Development System Data Sheet

CPLD	5M570	??? Defined by user code. EPT-Transfer-Demo code: 50mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA
Bus Transceivers	74LVC8245		30mA (All eight I/O's active)
USB Chip	FT2232H		60 mA (no sink current supplied to I/O's)
USB EEPROM	93LC56		2 mA (write current) 1 mA (read current)
66MHz Oscillator	CB3LV-3I-66M0		10 mA
Schmitt Buffer	74LVC1G17SE		1mA
User LEDs			20 mA
Total		50mA	175.5mA

*Theoretical Values only. This data needs to be validated

1.1.2 Core Board VUSB Power Budget

Device	Part Number	VUSB		
+1.8V Power Supply	MCP1725-1802E	70mA		
+3.3V Power Supply	MCP1725-3302E	215mA		
Total		285mA		

* Theoretical Values only. This data needs to be validated



CPLD Development System Data Sheet